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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,865	09/18/2003	Min-Su Kim	5484-110	8456

20575 7590 12/30/2005

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EXAMINER
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DOLAN, JENNIFER M

ART UNIT	PAPER NUMBER
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2813

DATE MAILED: 12/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<p style="text-align: center;"><b>Advisory Action</b> <b>Before the Filing of an Appeal Brief</b></p>	<b>Application No.</b> 10/666,865	<b>Applicant(s)</b> KIM, MIN-SU	
	<b>Examiner</b> Jennifer M. Dolan	<b>Art Unit</b> 2813	

**--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

THE REPLY FILED 02 December 2005 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☐ The period for reply expires \_\_\_\_\_ months from the mailing date of the final rejection.  
 b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

#### AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
 (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);  
 (b) ☐ They raise the issue of new matter (see NOTE below);  
 (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
 (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: \_\_\_\_\_. (See 37 CFR 1.116 and 41.33(a)).


4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
 5. ☒ Applicant's reply has overcome the following rejection(s): none.  
 6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
 7. ☐ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
 The status of the claim(s) is (or will be) as follows:  
 Claim(s) allowed: \_\_\_\_\_.  
 Claim(s) objected to: \_\_\_\_\_.  
 Claim(s) rejected: \_\_\_\_\_.  
 Claim(s) withdrawn from consideration: \_\_\_\_\_.

#### AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
 9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
 10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

#### REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because:  
See Continuation Sheet.  
 12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s). \_\_\_\_\_  
 13. ☐ Other: \_\_\_\_\_

  
**CARL WHITEHEAD, JR.**  
**SUPERVISORY PATENT EXAMINER**  
**TECHNOLOGY CENTER 2800**

Continuation of 11. does NOT place the application in condition for allowance because:

The Applicant first argues that the finality of the last office action was not proper. The Examiner disagrees, and points out that the newly applied rejections and references in the last office action were specifically applied to provide the newly claimed limitation that the insulation layer is disposed in contact with a sidewall of the gate line. As this limitation is substantially different from the previous claimed subject matter, in which the insulation layer merely needed to cover the gate line, the addition of a new reference to teach this newly claimed element is considered "necessitated by amendment."

The Applicant further argues that the SOI layers are located entirely in the active region, and no part of the SOI is disposed in the device isolation area. Hence, "it is incorrect to interpret Assaderaghi's shallow trench isolation regions as being included in, or part of, the SOI layer." This is not persuasive, because Assaderaghi clearly shows the STI regions disposed within the exact same layer as the SOI regions. Hence, it would be considered normal and proper to state that the STI regions are formed in the SOI layer. Assaderaghi additionally indicates that the SOI substrate is provided, and then STI structures are provided in that SOI layer, preferably with the bottom of the STI extending to the top of the buried oxide layer (see column 5, lines 43-62). Furthermore, it is not particularly relevant whether the STI structures of Assaderaghi are considered to be inside the SOI layer, since Assaderaghi, when combined with Chen, provides a structure in which a portion of the SOI layer remains underneath the isolation structure.

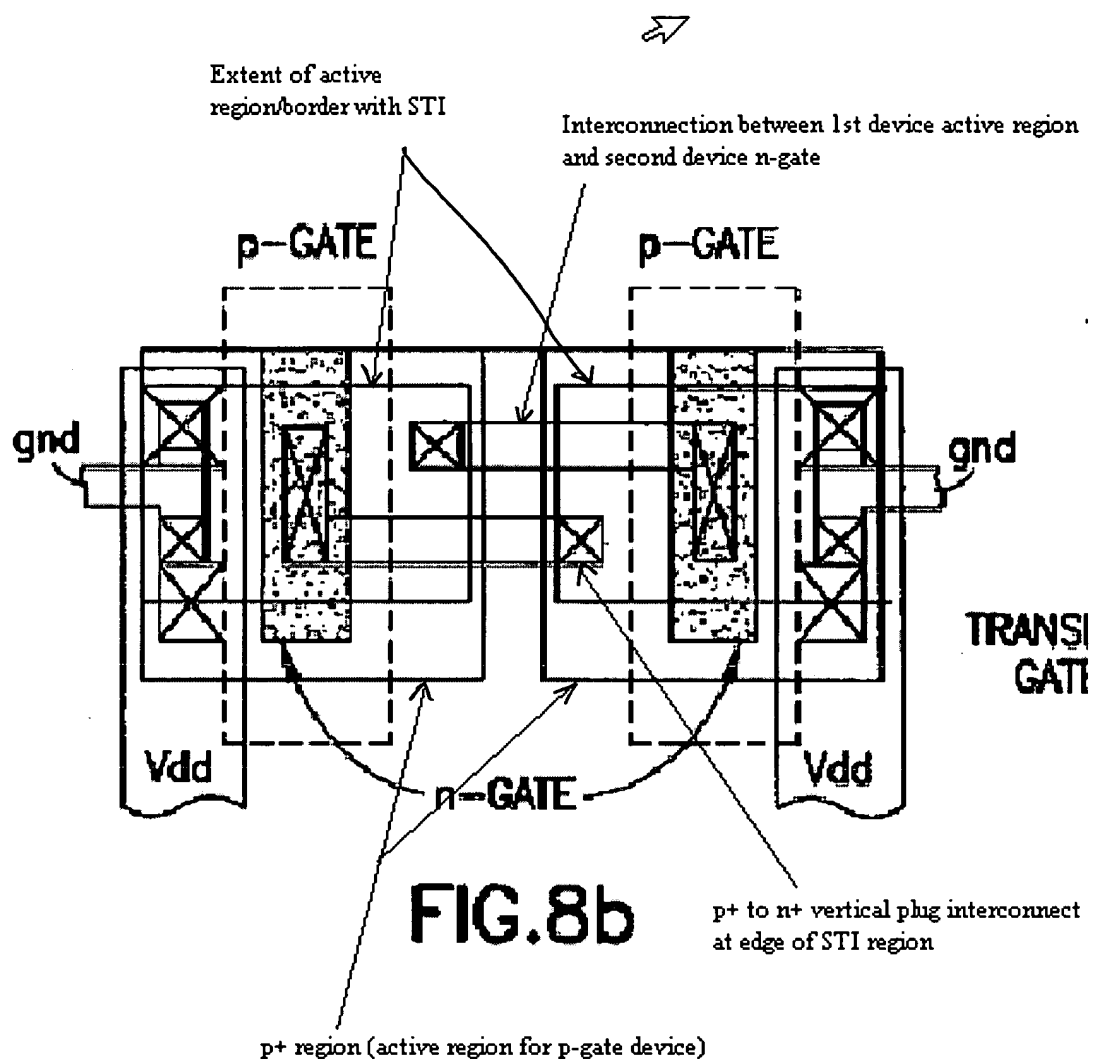
The Applicant further argues that the Applicant's specification and drawings illustrate a continuous SOI region, whereas Assaderaghi does not. The Examiner does not see the relevance of this issue, as such a feature is not specifically claimed, and is additionally present in the combination of Assaderaghi and Chen applied against claim 1.

The Applicant even further argues that the "left-most" n gate of fig. 8b is not disposed over the oxide isolation portion, and that it is not apparent in figure 8b where the active region is located. This is not persuasive, because the term "over" only requires that the feature be at a level higher than the active area and STI, rather than requiring any sort of overlap between the features. Furthermore, figure 7b directly shows and overlap between the n-gate and the active region. Similarly, since figures 7b and 8b show side and top views of the same area, it is apparent that the STI region includes an area directly under part of the n-gate (see attached figures).

The Applicant argues that the insulation layer in Assaderaghi is not contacting an upper surface of the active layer, but rather is disposed on top of the gate insulation layer. This is not persuasive, because Assaderaghi shows that the gate oxide layer is only present directly under the gate and the gate sidewalls (see figures 2, 3, 7). Hence, the isolation film contacts the upper surface of the source and drain regions, which are part of the active layer.

The Applicant further argues that Assaderaghi does not indicate that the stud interconnection 212 that rises vertically from the second gate line is part of the same interconnect structure as the stud interconnection 212 that rises vertically from the active region surrounding the first gate line. This is not persuasive, because figure 8b, which is the top view of the device of figure 7b, directly shows electrical connection between the second gate line and the first active region, as is stated in the previous office action.

The Applicant even further argues that there is no evidence in Assaderaghi that an LDD structure is present, such that the motivations for combining with Hills would apply. The Examiner disagrees, since Assaderaghi shows dopant regions that have a shape characteristic of regions including LDD portions, and further, Assaderaghi explicitly states that the device may include LDD regions (see column 12, lines 62-67). The Applicant is further reminded that since the Applicant's specification does not expressly or implicitly provide any purpose for the absence of the sidewall spacers, then the prior art teachings that it is known in the art and permitted to omit such layers is sufficient motivation for rejection.



Correspondence between figure 7B and figure 8B features